Training Opportunity for Portuguese Trainees

Reference	Title	Duty Station
PT-2019-TEC-EDM	**Space Microelectronics**	**ESTEC**

Overview of the Unit missions:

The trainee will be stationed at ESTEC/ESA in Noordwijk within the Microelectronics section of the Data Systems and Microelectronics division. The section cores responsibility covers the development of

(i) digital and analogue IP and microchips for space applications,
(ii) ASIC and FPGA radiation mitigation techniques
(iii) tools and methods for integrated circuits design and development.

The trainee will contribute substantially to one of the fields identified below, or a tailored set of objectives based on activities proposed below.

Overview of the field of activity proposed:

Within the field of space ASIC and FPGA microelectronics several different activities are proposed and described below:

a) Perform benchmarking of existing digital IP Cores on the new European BRAVE FPGAs, while at the same time helping to identify areas of improvement for the programming tools. Develop and test functional representative cases of Software Defined Hardware with BRAVE NG-LARGE FPGA, implementing on-board data processing functions that are representative payload functions, exploiting the main new elements that differentiate BRAVE LARGE from MEDIUM: DDR i/f, SerDes and embedded CPU.
b) Evaluate the effectiveness of the existing suite of space FPGA mitigation tools and techniques (SETA for Single Event Transients for the Microsemi RTG4 FPGA, STAR/RoRA/VPLACE for SEEs in Xilinx FPGAs) with the FPGA radiation sensitivity analysis tools (FT-UNSHADES2/FLIPPER fault injection tools) and determine in terms of SEE rates their radiation performance. The target FPGA technologies include Microsemi RTG4, Xilinx Virtex-4 and Virtex-5.

c) Create a compiler LLVM (**Low Level Virtual Machine)** back-end for the SPARC LEON2/3 and/or the current space micro-controller core identified and extensively test it on the space grade FPGA image.

d) Perform microelectronics design and test of analogue and mixed-signal new IP cores and devices for space applications. ESA would like to finish the design of a maximum power point tracker (MPPT) new analogue IP core design (that will be then manufactured with the Microchip Atmel CMOS SOI 150nm technology and tested), and in addition, there are a few recently manufactured mixed-signal chips that need to be functionally and electrically tested and characterised in our laboratory. These chips include Single Event Transient (SET) test vehicles, a CAN bus high voltage transceiver, ADCs, DACs and other analogue IPs, all of them manufactured with a the IMEC DARE technology. Additionally the porting of these mixed-signal IP to IHP, XFAB and ST technology needs to be investigated.

e) Investigate a digital IP Cores database structure, and develop the necessary tools so that the entire flow, from configuration to final implementation can be automated, enabling the generation of occupancy and performance estimations for several FPGA devices, such as BRAVE, RTG4 or Xilinx Kintex Ultrascale.

f) Improve usability of the SoCRocket Virtual Platform, integrating models of SystemC IP Cores, and using the platform to solve an on-board data processing problem exploring different possible SoC architectural solutions.

Required Education:

Applicants should have just completed (not more than three years ago) or be in their final year of a university course at Master's level in Microelectronics, with special interest in digital and/or analogue VLSI design and technology, and:

- Knowledge / experience with C, C++ and digital VHDL design tools (e.g. MENTOR, SYNOPSYS) or/and
- Knowledge / experience with analogue VLSI design tools (e.g. CADENCE, MENTOR) or/and
- Knowledge / experience with electrical tests of VLSI components

Knowledge / experience with radiation effects on semiconductors would be a valuable asset
Candidates must be fluent in written and spoken English