Training Opportunity for Portuguese Trainees

Reference	Title	Duty Station
PT-2016-TEC-EDM	**Space Microelectronics**	**ESTEC**

Overview of the Unit missions:

The trainee will be stationed at ESTEC/ESA in Noordwijk within the micro-electronics section of the space data-handling division. The section responsibility covers the development of (i) digital and analogue IP for space applications, (ii) ASIC and FPGA radiation mitigation techniques and (iii) tools for microelectronics design and development. The trainee will contribute substantially to one of the fields identified in a) digital IP cores for the space community, b) FPGA radiation mitigation techniques, c) processor programming tools and d) analogue and mixed-signal IP core design and testing

Overview of the field of activity proposed:

Within the field of space ASIC and FPGA microelectronics four different activities are proposed and described below:

a) Develop the VHDL RTL for a radiation tolerant DDR2/3 SRAM memory controller as IP block as complement to the ESA IP core offering for both FPGA and ASIC, including the digital radiation mitigation techniques. Synthesise it to Microsemi ProASIC3, Xilinx Virtex-5 FPGA and the 65nm CMOS ASIC target technology. Test the FPGA images in the laboratory with space grade DDR2/3 SRAM memories.

b) Evaluate the effectiveness of the suite of space FPGA mitigation tools and techniques (SETA for Single Event Transients for the Microsemi ProASIC3 FPGA, STAR/RoRA/VPLACE for SEEs in Xilinx FPGAs) with the FPGA radiation sensitivity analysis tools (FT-UNSHADES2/FLIPPER fault injection tools) and determine in terms of SEE rates their radiation performance. The target FPGA technologies include Microsemi ProASIC3, Xilinx Virtex-4 and Virtex-5. The Atmel AT40K family might be addressed depending on the Atmel tools status.

c) Create a compiler LLVM back-end for the SPARC LEON2/3 and/or the current space micro-controller core identified and extensively test it on the space grade FPGA image.

d) Perform microelectronics design and test of analogue and mixed-signal new IP cores and devices for space applications. ESA would like to finish the design of a maximum power point tracker (MPPT) new analogue IP core design (that will be then manufactured with the Atmel technology and tested), and in addition, there are a few recently manufactured mixed-signal chips that need to be functionally and electrically tested and characterised in our laboratory. These chips include Single Event Transient (SET) test vehicles, a CAN bus high voltage transceiver, ADCs, DACs and other analogue IPs, all of them manufactured with a the IMEC DARE technology. Additionally the porting of these mixed-signal IP to IHP, XFAB and ST technology needs to be investigated.

Required Education:

Applicants should have just completed (conclusion not older than two years) or be in their final year of a university course at Master's level in Microelectronics, with a special interest in analogue VLSI design and technology
Knowledge / experience with C, C++ and digital VHDL design tools (e.g. NEMTOR, SYNOPSYS) or/and
Knowledge / experience with analogue VLSI design tools (e.g. CADENCE, MENTOR) or/and
Knowledge/ experience with electrical tests of VLSI components
Knowledge / experience with radiation effects on semiconductors would be an asset
Candidates must be fluent in English or French, the official languages of the agency