Sample Project: Electronics design: VFAT3 test bench developer.

Code	PH2464
Programme	TRAIN-PTES
Department	PH
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Title

Electronics design: VFAT3 test bench developer.

Description

VFAT3 is a complex mix signal (analog and digital) ASIC currently under design for the front-end readout of new GEM detectors within CMS. The trainee position would focus on the development of a test environment for the ASIC. Initially this would require verilog simulation using cadence design tools. This would be followed by PCB design and firmware design.

The trainee would work within a group of design engineers and be supervised by a CERN engineer.

Skills

Low and High Frequency Engineering: Measurement techniques. Networks and Systems: Integrated circuits, Sensors. Programming Languages: C++. Theory of Electrical Engineering: Modeling and simulation Analog and/or digital design, pcb design, FPGA firmware, verilog or VHDL, use of CAD design tools such as Cadence

Disciplines

Information Technologies, Electrical Engineering