Training Opportunity for Portuguese Trainees

Reference	Title	Duty Station
PT-2013-TEC-EDM(2)	**Evaluation and Customization of SPARC development tools**	**ESTEC**

Overview of the Unit missions:

The unit of destination of the trainee is TEC-EDM, microelectronics section.
The section is in charge of providing ASIC and FPGA technical support to ESA projects and of undertaking and coordinating R&D activities for new microelectronic technologies, including EDA tools, IP Cores, design methodology, HW-SW co-design, ASIC digital and analogue libraries, etc. The section has lead and is leading the development of various types of SPARC-V8 based space qualified micro-processors.

Overview of the field of activity proposed:

The activity will mainly focus on the enhancement of existing tools supporting software development for LEON-based systems, including, if necessary, the design of new tools.
Two applications will be mainly targeted:

- Compiler, adding to newest releases of the GCC compiler the capability to generate code targeted to LEON2-based systems; an assessment of the performance improvements over the use of older compiler releases will, then, be performed.
- Debugging and monitoring tools, focusing on interfacing with all LEON families (including the newly developed multi-core LEON4 system), providing access to all their introspective capabilities.
  Particular focus shall be devoted on the possibility of the integration with external development environments (e.g. Eclipse IDE) and/or Open Source tools (e.g. GDB) and of its extension to accommodate future needs.

Overall this part of the activity main focus will be on the LEON2 architecture, as tools necessary to use/control/debug/monitor it are not any more supported by the industry.
An in depth knowledge of the LEON 2 architectures will be required to carry out this part of the activity and it will be acquired mainly by study of the VHDL code implementing such architectures.

The tools enhanced/designed in the steps outlined above shall then be used to benchmark and characterize (some of) the LEON-based systems developed or being developed at the Agency.

An analysis of processors and micro-controller OpenSource and commercial debugging and monitoring tools will be required before the start of the project, in order to get familiar with the technology and to consolidate the requirements to be applied to the corresponding tools for LEON-based systems.

Given the nature of the project and the close interaction of the microelectronic section with the software division (TEC-SW), the trainee will be required to interface with its members in order to properly carry out the project.

Required Education:

Applicants should have just completed, or be in their final year of a University course at Masters level in Electrical or Computer Engineering. A strong background in Software Engineering and C/C++ programming is required and knowledge of Hardware Description Languages (mainly VHDL) is welcome.
Candidates must be fluent in English and/or French, the official languages of the Agency.
Candidates should have a high degree of autonomy together with an attitude to work in an international team environment. They should have good communication skills and an interest into innovative technologies.