Training Opportunity for Portuguese Trainees

Reference	Title	Duty Station
PT-2013-TEC-EDM(3)	**Evaluation of FPGA mitigation techniques**	**ESTEC**

Overview of the Unit missions:

The unit of destination of the trainee is TEC-EDM, microelectronics section.
The section is in charge of providing ASIC and FPGA technical support to ESA projects and of undertaking and coordinating R&D activities for new microelectronic technologies, including EDA tools, IP Cores, design methodology, HW-SW co-design, ASIC digital and analogue libraries, etc. The section has lead and is leading design mitigation techniques against radiation for FPGAs.

Overview of the field of activity proposed:

Non radiation-hardened FPGAs (that is, Radiation-tolerant or even COTS FPGAs), are already being used in some space applications because of their added value in higher performance or lower power consumption. There are currently no commercial tools available to provide the FPGA designers information to assess and optimise a design according to its radiation behaviour.

Two TEC-EDM activities have recently provided 2 tools in that context: SETA for the Microsemi ProASIC3 FPGA and FT-UNSHADES2 providing fault injection for designs targeting both FPGAs and ASICs. Later in 2013 two other tools will receive major updates: a newer version or STAR/RoRA/VPLACE will support Virtex-5 FPGAs and the FLIPPER fault injection tool will support Virtex-4.

The work will focus on evaluating these different mitigation tools that have been recently provided to the Avionics Lab. Each tool will be evaluated separately as well as in combination in order to have a complete workflow solution addressing each FPGA technology.

The target FPGA technologies include Microsemi ProASIC3, Xilinx Virtex-4 and Virtex-5. The Atmel AT40K family might be addressed depending on the Atmel tools status.

Several test designs will be used in the exercise: the selection will be done at the beginning of the activity according to the status at that time. The design candidates will be among the already existing ESA-IP Cores, TEC-EDM internal designs and microcontroller-based designs; but other potential designs coming from industry will be considered if available.

It is expected to work in collaboration with the research groups that have provided the tools: Politecnico di Torino, Politecnico di Milano and University of Seville.

Collaboration with other sections within the TEC-ED division as well as TEQ-QEC is expected.

Required Education:

Applicants should have just completed, or be in their final year of a University course at Masters level in Electrical or Computer Engineering. A strong background in digital microelectronics, including Hardware Description Languages (for instance VHDL), is required and knowledge of programming languages as C/C++ is welcome.
Candidates must be fluent in English and/or French, the official languages of the Agency.
Candidates should have a high degree of autonomy together with an attitude to work in an international team environment. They should have good communication skills and an interest into innovative technologies.